3D INTEGRATED CIRCUITS

BY

Abstract

Unlike conventional electronic circuits, where transistors are placed in a single plane, three-dimensional (3D) integrated circuits utilize multiple tiers of active devices, placed one above another. Recent advances in processing technologies have brought these technologies into the realm of achievable reality, and today, several academic, corporate and government labs run fabrication processes for building 3D integrated circuits. The move to the third dimension immediately provides increased packing densities per unit footprint, and provides a path for maintaining Moore's law rates of growth at the system level, even as questions are being raised about the sustainability of device-level scaling. 3D circuits offer numerous other advantages as well, including the potential for reduced interconnect lengths, and the ability to easily integrate heterogeneous technologies on multiple tiers into a single package.

The use of three dimensional chip fabrication technologies has emerged as a solution to the difficulties involved with the continued scaling of bulk silicon devices. While the technology exists, it is undervalued and underutilized largely due to the design and
Verification challenges a complex 3D design presents.

This work presents an

1. introduction to 3D IC's ,
2. motivation ,
3. architecture performance characteristics,
4. standard cell tool design,
5. introduction to global routing
6. Hierarchical global routing for three dimensional integrated circuits (3DIC).

Keywords: Timing, energy performance, standard tool design, illustration of bisection, global routing, 3-D magic.

Conclusion

- 3D IC design is a relief to interconnect driven IC design.
- Still many manufacturing and technological difficulties
- Needs strong EDA applications for automated design

Introduction

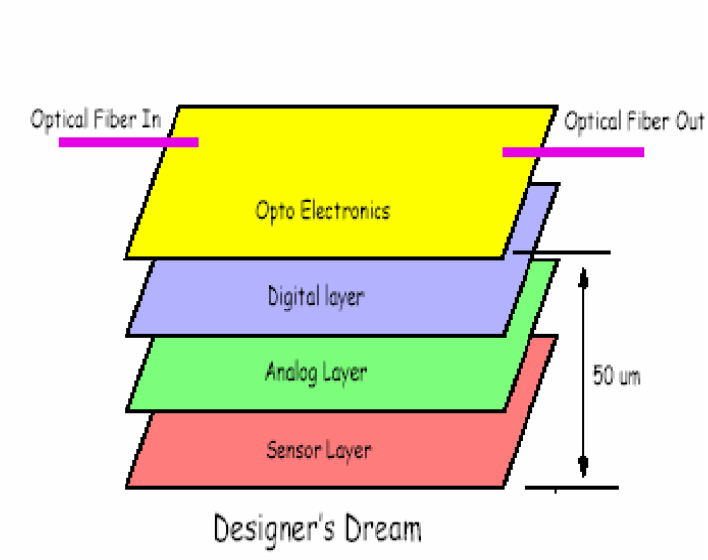
There is a saying in real estate; when land get expensive, multi-storied buildings are the alternative solution. We have a similar situation in the chip industry. For the past thirty years, chip designers have considered whether building integrated circuits multiple layers might create cheaper, more powerful chips.

Performance of deep-sub micrometer very large scale integrated (VLSI) circuits is being increasingly dominated by the interconnects due to increasing wire pitch and increasing die size. Additionally, heterogeneous integration of different technologies on one single chip is becoming increasingly desirable, for which planar (2-D) ICs may not be suitable.

The three dimensional (3-D) chip design strategy exploits the vertical dimension to alleviate the interconnect related problems and to facilitate heterogeneous integration of technologies to realize system on a chip (SoC) design. By simply dividing a planar chip into separate blocks, each occupying a separate physical level interconnected by short and vertical interlayer interconnects (VILICs), significant improvement in performance and reduction in wire-limited chip area can be achieved. In the 3-Ddesign architecture, an entire chip is divided into a number of blocks, and each block is placed on a separate layer of Si that are stacked on top of each other.

What is a 3D Integrated Circuit?

• A 3D chip is comprised or 2 or more layers of
Semiconductor devices which have been thinned, bonded together, and interconnected to form a "monolithic" circuit.
• Frequently, the layers (also called tiers) are comprised of devices made in different technologies.



Why Consider 3D Now?

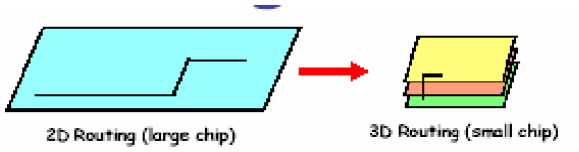
• The move to 3D is being driven entirely by Industry needs.

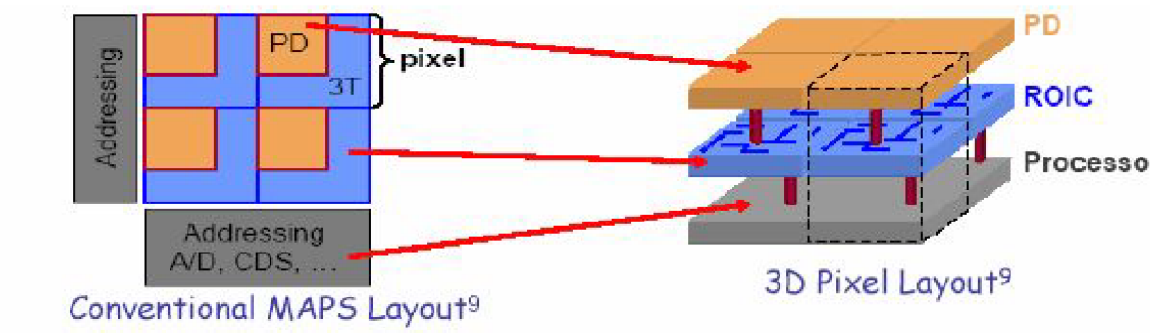
– In submicron processes, RC delay is a limiting factor in performance improvement.

– Low k dielectrics to reduce C have been difficult to implement.

– Circuit overhead is taking a larger fraction of the chip area.

• 3D is discussed in the ITRS (International Technology Roadmap for Semiconductors) as an approach to improve circuit performance and permit continuation of Moore's Law.





Motivation For 3-D ICs

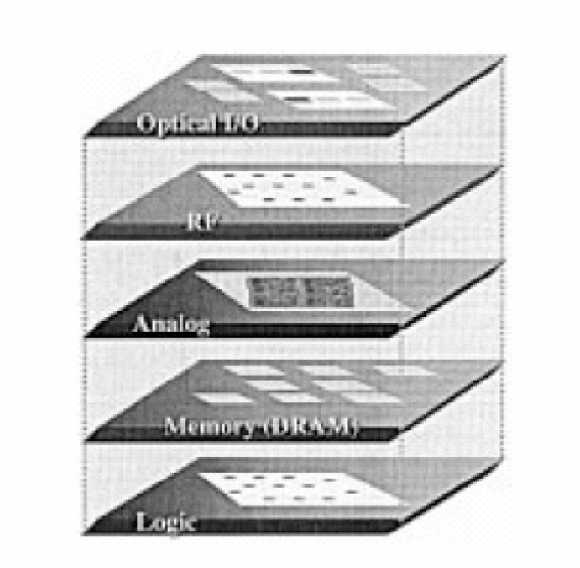
The unprecedented growth of the computer and the information technology industry is demanding Very Large Scale Integrated (VLSI) circuits with increasing functionality and performance at minimum cost and power dissipation. Continuous scaling of VLSI circuits is reducing gate delays but rapidly increasing interconnects delays. A significant fraction of the total power consumption can be due to the wiring network used for clock distribution, which is usually realized using long global wires.

Furthermore, increasing drive for the integration of disparate signals (digital, analog, RF) and technologies (SOI, SiGe, GaAs, and so on) is introducing various SoC design concepts, for which existing planner (2-D) IC design may not be suitable.

3D Architecture

Three-dimensional integration to create multilayer Si ICs is a concept that can significantly improve interconnect performance ,increase transistor packing density, and reduce chip area and power dissipation. Additionally 3D ICs can be very effective large scale on chip integration of different systems.

In 3D design architecture, and entire (2D) chips is divided into a number of blocks is placed on separate layer of Si that are stacked on top of each other. Each Si layer in the 3D structure can have multiple layer of interconnects (VILICs) and common global interconnects.



Performance Characteristics

- Timing
- Energy
- With shorter interconnects in 3D ICs, both switching energy and cycle time are expected to be reduced

Energy performance

- Wire length reduction has an impact on the cycle time and the energy dissipation
- Energy dissipation decreases with the number of layers used in the design
- Following graphs are based on the 3D tool described later in the presentation

Energy performance graphs

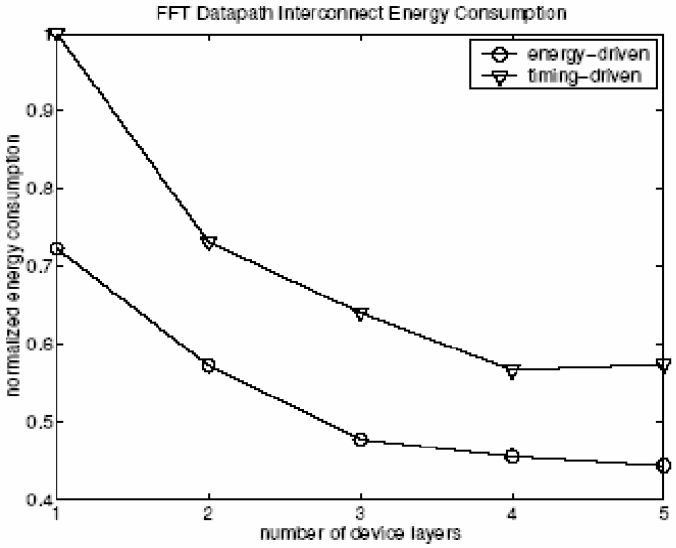


Figure 4: Interconnect energy consumption of the FFT datapath vs. number of wafers used for placement.

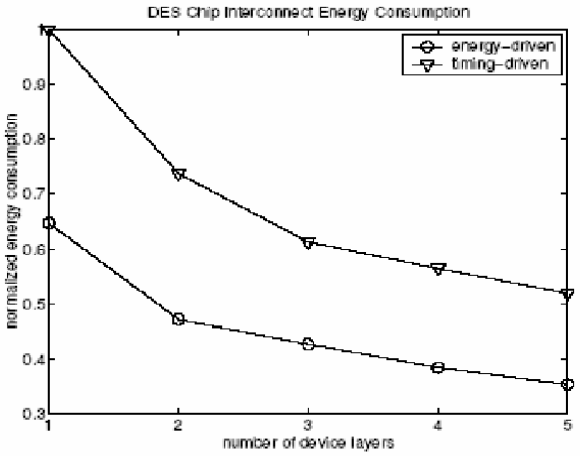


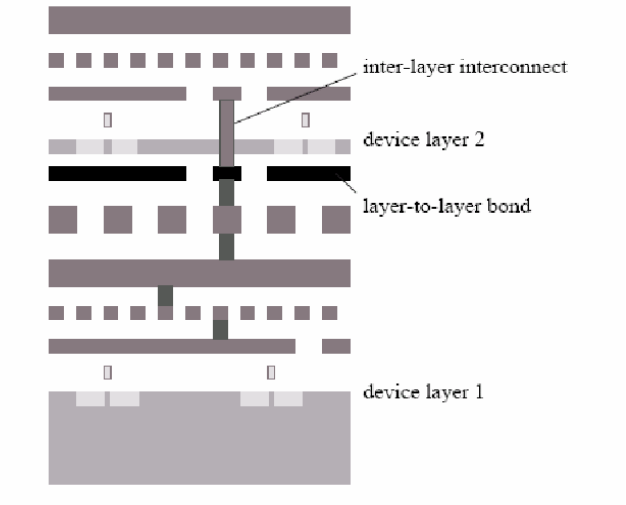
Figure 5: Interconnect energy consumption of the DES chip vs. number of wafers used for placement.

3D Standard Cell tool Design

- 3D Cell Placement
  -Placement by min-cut partitioning
- 3D Global Routing
  -Inter-wafer vias
- Circuit layout management
  -MAGIC

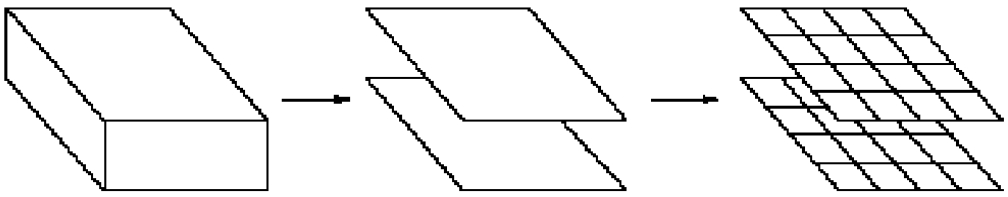
3D Standard Cell Placement

- Natural to think of a 3D integrated circuit as being partitioned into device layers or planes
- Min cut partitioning along the 3rd dimension is same as minimizing vias

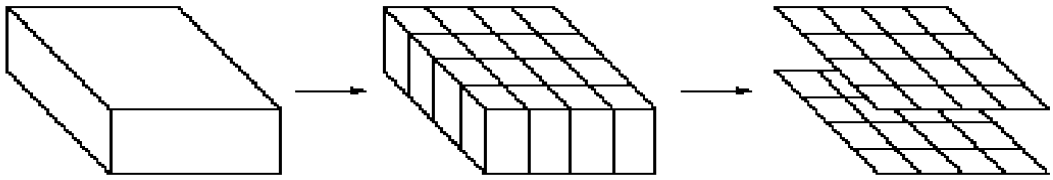


Total wire length vs. Vias

- Can trade off increased total wire length for fewer inter-plane vias by varying the point at which the design is partitioned into planes
- Plane assignment performed prior to detailed placement
- Yields smaller number of vias, but greater overall wire length



- Plane assignment not made until detailed placement stage
- Yields smaller total wire length but greater number of vias



Intro to Global Routing

→Overview

→Global Routing involves generating a "loose" route for each net.

→Assigns a list of routing regions to a net without actually specifying the geometrical layout of the wires.

→Followed by detailed routing

→Finds the actual geometrical shape of the net within the assigned routing regions.

→Usually either sequential or hierarchical algorithms.

Hierarchical Global Routing

→ Tool uses a hierarchical global routing algorithm

→ Based on Integer programming and Steiner trees

→Integer programming approach still too slow for size of problem and complexity (NP-hard)

→Hierarchical routing methods break down the integer program into pieces small enough to be solved exactly

2D Global Routing

→A 2D Hierarchical global router works by recursively bisecting the routing substrate.

→Wires within a Region are fully contained or terminate at a pin on the region boundry.

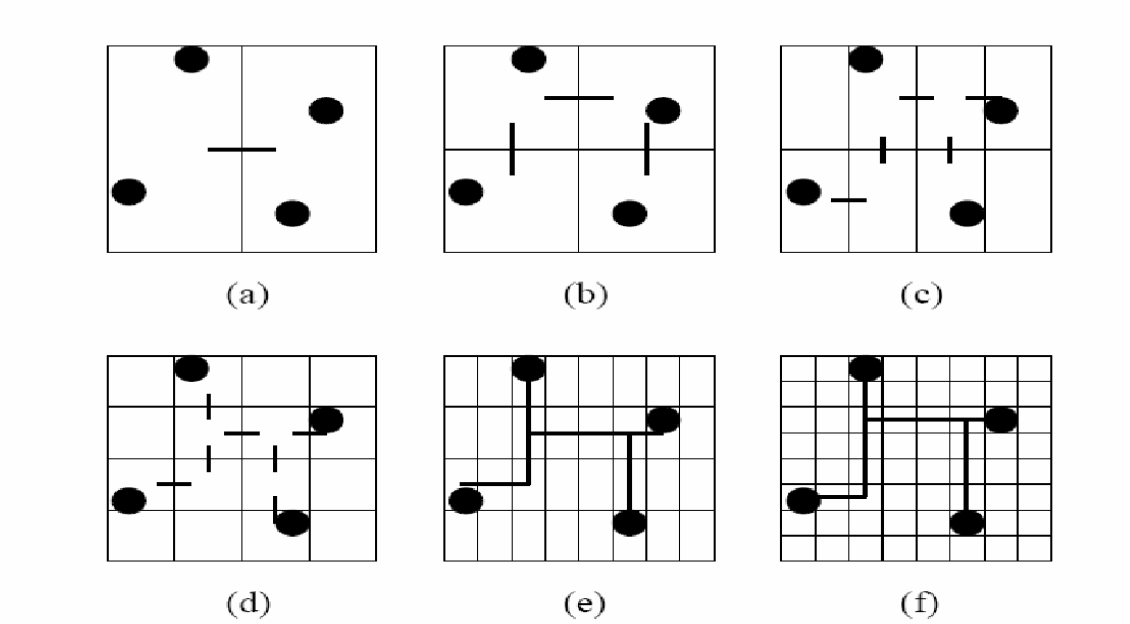
→At each partitioning step the pins on the side of the routing region is allocated to one of the two sub regions.

→Wires Connect cells on both sides of the partition line.

→These are cut by the partition and for each a pin is inserted into the side of the partition

→Once complete, the results can be fed to a detailed router or switch box router (A switchbox is a rectangular area bounded on all sides by blocks)

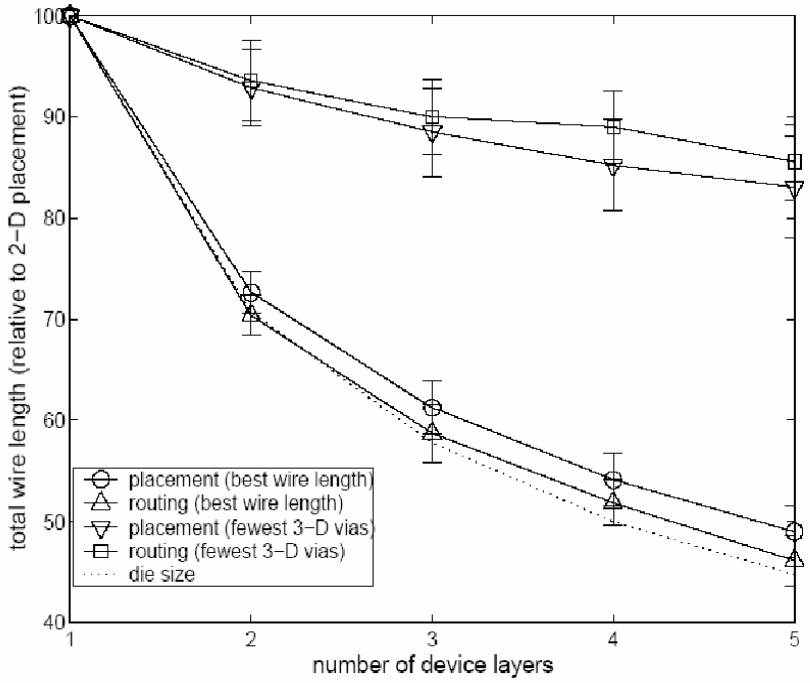
Illustration of Bisection



Extending to 3D

→Routing in 3D consists of routing a set of aligned congruent routing regions on adjacent wafers.
→Wires can enter from any of the sides of the routing region in addition to its top and bottom
→3D router must consider routing on each of the layers in addition to the placement of the inter-waver vias
→Basis idea is: You connect a inter-waver via to the port you are trying to connect to, and route the wire to that via on the 2D plane.
→All we need now is enough area in the 2D routing space to route to the appropriate via

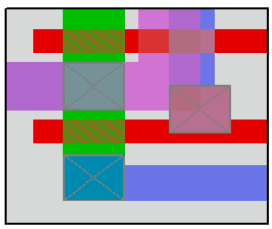
3D Routing Results



Percentage Of 2D Total wire Length
Minimizing for Wire Length:
2 Layers ~ 28%
5 Layers ~ 51 %

Minimizing for via count:
2 Layers ~ 7%
5 Layers ~ 17%

3D-MAGIC



- MAGIC is an open source layout editor developed at UC Berkeley
- 3D-MAGIC is an extension to MAGIC by providing support for Multi-layer IC design
- What's different
  - New Command :bond
  - Bonds existing 2D ICs and places inter-layer Vias in the design file
  - Once Two layers are bonded they are treated as one entity

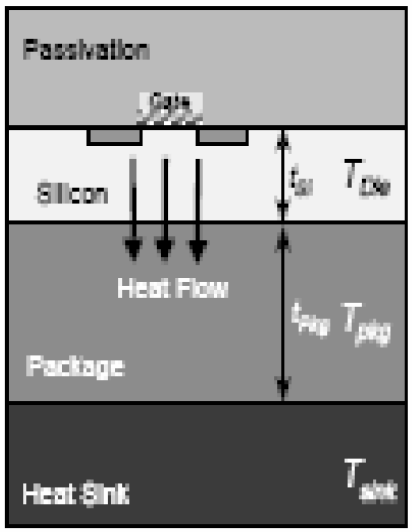
Concerns in 3D circuit

- Thermal Issues in 3D-circuits
- EMI
- Reliability Issues

Thermal Issues in 3D Circuits

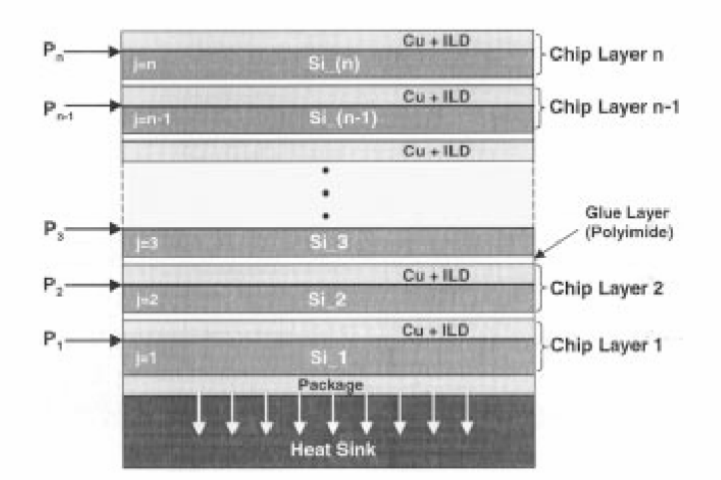
- Thermal Effects dramatically impact interconnect and device reliability in 2D circuits
- Due to reduction in chip size of a 3D implementation, 3D circuits exhibit a sharp increase in power density
- Analysis of Thermal problems in 3D is necessary to evaluate thermal robustness of different 3D technology and design options.

Heat Flow in 2D



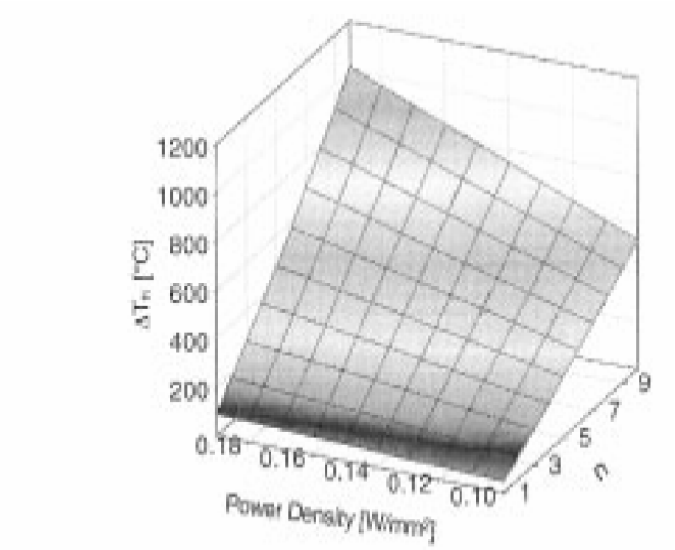
Heat generated arises due to switching in 2D circuits we have only one layer of Si to consider.

Heat Flow in 3D



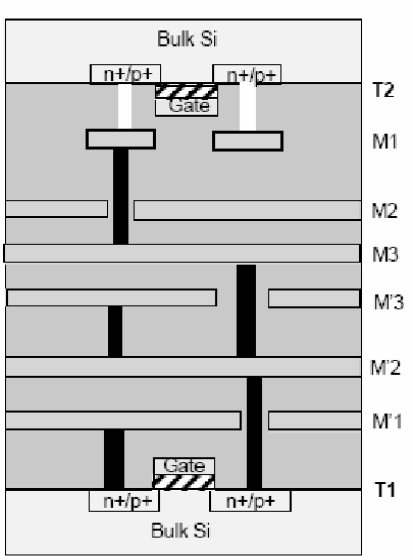
With multi-layer circuits , the upper layers will also generate a significant fraction of the heat.

Heat increases linearly with level increase



EMI in 3D ICs

- Interconnect Coupling Capacitance and cross talk
  - Coupling between the top layer metal of the first active layer and the device on the second active layer devices is expected



EMI

- Interconnect Inductance Effects
  - Shorter wire lengths help reduce the inductance
  - Presence of second substrate close to global wires might help lower inductance by providing shorter return paths

Reliability Issues?

- Electro thermal and Thermo-mechanical effects between various active layers can influence electro-migration and chip performance
- Die yield issues may arise due to mismatches between die yields of different layers, which affect net yield of 3D chips.

Conclusion

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- Still many manufacturing and technological difficulties
- Needs strong EDA applications for automated design